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(54) Insulated gate bipolar transistor.

(57) An insulated gate bipolar transistor (IGBT) permits a large current to uniformly flow. A plurality of single crystal island regions (61) are formed in a supporting substrate (2) using dielectric films (1). Formed in each of the island regions are an n^- first region (61), a p second region (41) within the first region, an n^+ third region (32) within the second region (41) and a p^{++} fourth region (11) between the first region (61) and the dielectric film. All of these regions are exposed to the surface of the island region. Formed on the surface of the island region are a first main electrode (E) kept in ohmic contact with the second (41) and third (32) regions, a second main electrode (C) kept in ohmic contact with the fourth region (11) and a control electrode (G) located on the second (41) and third region (32) through an insulator (6).

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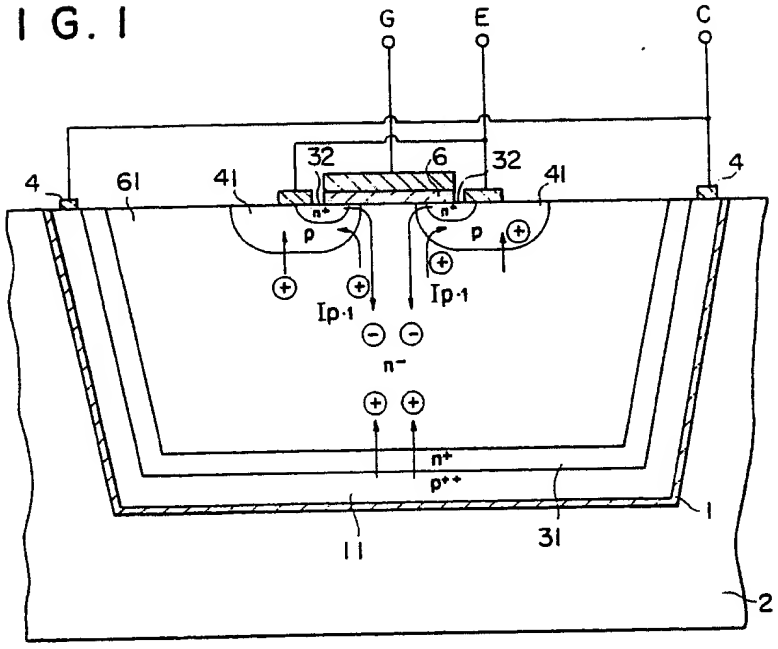
FIG. 1



SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device and more particularly to a semiconductor device that is suitable for integration.

In recent years, an insulated gate bipolar transistor (hereinafter referred to as IGBT) has attracted considerable attention as a semiconductor device that is capable of controlling relatively large current.

One example of the conventional IGBT structures is disclosed in JP-A-57-120369 in which one main electrode (cathode) and a control electrode are formed on the main surface of a substrate whereas the other main electrode (anode) is formed on the bottom surface of the substrate. Such a structure is difficult to integrate along with several other devices on the same substrate since the main electrodes are formed on both surfaces of the substrate.

It is desired for integration to form all three terminals of IGBT on the same surface. Such a lateral IGBT structure is proposed in USP 4,364,073 and JP-A-59-132667. Fig. 9 shows this structure.

As seen from Fig. 9, an p^-layer 41 is formed in an n^--layer 61 that is formed in an p^--semiconductor substrate 71, and further an n^+-layer 32 is formed in p^- layer 41. Formed in n^--layer 61 is a p^+-layer 13 distinatly from p^-layer 41. N^+-layer 32 and p^-layer 41 are short-circuited by an emitter electrode. A gate electrode 6 is provided on part of the surface of p^- layer 41 through a gate insulating film in such a way that it covers parts of n^+-layer 32 and n^--layer 61. The provision of p^+-layers 14 serves to electrically separate that device in issue from the other devices formed in the same substrate.

In the operation of the semiconductor device of Fig. 9, when a positive potential is applied to gate electrode 6, p^-layer 41 below gate insulating film 3 is inverted to form a channel. Then, electrons (indicated by ⊖ in Fig. 9) flowed out from n^+-layer 32 reach p^+layer 13 through the channel and n^--layer 61. This injects holes (indicated by ⊕ in Fig. 9) from p^+-layer 13 into n^--layer 61. Thus, the conductivity of n^--layer 61 of high resistance is modulated so as to cause n^--layer 61 to have low resistance. Accordingly, the IGBT of Fig. 9 has advantages that its resistance loss is little and also its power consumption is little since it is an insulated gate semiconductor device.

However, the lateral IGBT structure of Fig. 9 has the following disadvantages. Since p^+-layer 13 is provided only in the substrate surface, the electrons ⊖ flowed out from n^+-layer 32 and the holes ⊕ injected from p^+-layer 13 flow only in the lateral direction in n^--layer 61. Thus, the conductivity modulation of n^-- layer 61 occurs only in the neighborhood of its surface so that large current can not flow. Further, since the holes ⊕ flow concentratively in the lateral direction immediately below n^+-layer 32 so that a potential drop occurs due to the lateral resistance component R in p^-layer 41. This potential drop foward-biases n^+-layer 32 to inject electrons. Thus, a thyristor composed of n^+-layer 32, p^-layer 41, n^--layer 61 and p^+-layer 13 will be turned on (so-called "latch-up" occurs), thereby making it impossible to control current by means of a gate.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an IGBT structure semiconductor device that can be integrated and permits a large current to uniformly flow therethrough.

The above object can be achieved by adopting a structure in which the direction of a main current in IGBT is changed plural times (i.e. the main current flows in the lateral direction in a channel region of IGBT, flows in the vertical direction in a drift region thereof and flows towards one main surface of the substrate in a collector region thereof). In other words, the above object can be attained by a structure that IGBT having a passage through which the main current flows in the vertical direction (vertical with respect to the main surface) is formed within a single crystal island surrounded by an insulating film in the substrate.

In order to attain the above object, in accordance with the present invention, there is provided a semiconductor device comprising a single crystal island region surrounded by an electric insulating means in a substrate, said single crystal island region including a fourth semiconductor region of one conduction type, a first semiconductor region of the other conduction type formed in the fourth semiconductor region, a second semiconductor region of one conduction type formed in the first semiconductor region and a third semiconductor region of the other conduction type formed in the second semiconductor region, the first to fourth semiconductor regions being exposed to the same main surface; one main electrode on the main surface which is connected with the fourth semiconductor region; the other main electrode on the main surface which is connected with both the second semiconductor region and the third semi-

conductor region; and an insulated gate control electrode provide on the main surface of the second semiconductor region and extended over the first semiconductor region and the third semiconductor region.

The semiconductor device in accordance with the present invention has the following advantages. Since a collector region can be formed so as to surround an island-shaped drift region, a main current can be passed in an large amount and unformly through the drift region in its vertical direction. Moreover, the carriers injected from the collector region flow in the drift region in its vertical direction so that the amount of carriers flowing in the lateral direction below an emitter layer is reduced, thereby obviating the problem of "latch-up".

Further, respective electrodes can be extracted out from one surface of the substrate so that the semiconductor device which can be easily integrated can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a vertical sectional view of a first embodiment of the present invention;

Fig. 2 is a vertical sectional view of a second embodiment of the present invention;

Fig. 3 is a vertical sectional view of a modification of the second embodiment;

Fig. 4 is another modification of the second embodiment;

Fig. 5 is still another modification of the second embodiment;

Fig. 6A is a vertical sectional view of a third embodiment of the present invention;

Fig. 6B is a sectional view taken on line a-a' of Fig. 6A;

Fig. 7A is a vertical sectional view of a modification of the third embodiment;

Fig. 7B is a sectional view taken on line a-a' of Fig. 7A;

Fig. 8A is a vertical sectional view of a further modification of the second embodiment of the present invention;

Fig. 8B is a sectional view taken on line a-a' of Fig. 8A; and

Fig. 9 is a vertical sectional view of the prior art of IGBT.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now referring to the drawings, several embodiments of the present invention will be explained below. Fig. 1 is a vertical sectional view of a first embodiment of the present invention. An n^--single-crystal island 61 is formed in a polycrystal semiconductor layer 2 which is a supporting substrate. n^--single-crystal island 61 is dielectrically isolated from the other single crystal islands by an electric insulating means, e.g. an insulating film 1 of SiO_2. A p^{++}-layer 11 and n^+ layer 31 are formed between n^- single crystal island 61 and inter-layer film 1 so as to surround n^- single crystal island 61. A collector electrode 4 is attached to the surface of p^{++} layer 11. A MOS gate consisting n^+ layers 32, p layers 41 and an insulating film 6 is formed in n^- single crystal island 61. If a positive potential is applied to a gate electrode G on gate insulating film 6, p layer 41 immediately below gate insulating film 6 is inverted in its conduction type, and electrons $\ominus$ flowed out from n^+ layer 31 drift through n^- single crystal island 61 in the vertical direction to reach p^{++} layer 11. Further, the electrons $\ominus$ flow into p^{++} layer 11 through n^+ layer 31 so that holes $\oplus$ are injected from p^{++} layer 11 into n^+ layer 31, thus producing the conductivity modulation in the device.

The device of Fig. 1 has the following advantages over the conventional lateral IGBT. First, the device of Fig. 1 has a current path through current flows in the vertical (longitudinal) direction with respect to the substrate main surface. Secondly, the conductivity modulation occurs in the vertical direction so that a large current is permitted to flow uniformly. Thirdly, holes $\oplus$ flow in the vertical direction so that the hole current laterally flowing through p layer 41 immediately below n^+ layer 32 is reduced whereby the device is hardly latched up.

Incidentally, Fig. 1 is a vertical sectional view of an actual device. In the actual device, respective elements (devices) are arranged to be extended in the direction perpendicular to the sheet. Further, a great number of such extended elements are arranged in one single crystal island 61 in such a manner as shown in Figs. 2 and 7A with respect to one single crystal island 61. This applies to the respective embodiments of Figs. 3, 4, 5, 6A and 8A.

Fig. 2 is a vertical sectional view of a second embodiment of the present invention. In Fig. 2, the same reference symbols as in Fig. 1 refer to the same or equivalent parts in Fig. 1. The structure of this embodiment is different from that of Fig. 1 in that p^{++} layer 11 and n^+ layer 31 are short-circuited by collector electrode 4 in their surface. In this structure, a part of the electrons flowed through n^- layer 61 flow into collector 4 via n^+ layer 31 so that injection of holes from p^{++} layer 11 is restricted thereby preventing the latch-up, and excess electrons can be extracted out from n^+ layer 31, thereby permitting the device to be turned off at a high speed.

Fig. 8A is a vertical sectional view of a modification of the second embodiment of the present invention. Fig. 8B is a sectional view taken on line a-a′ of Fig. 8A. In Figs. 8A and 8B, the same reference symbols as in Fig. 1 refer to the same or equivalent parts in Fig. 1. The structure of this modification is different from that of the embodiment of Fig. 2 in that n^+ layer 31 is partially removed so that p^+ layer 11 and n^- single crystal island 61 are partially connected with each other. In Fig. 2, p^{++} layer 11 is completely covered with n^+ layer 31 so that the injection efficiency of holes from p^{++} layer 11 may be so low as to make the conductivity modulation insufficient. On the other hand, in the modification of Figs. 8A and 8B, n^+ layer 31 is partially removed so that p^{++} layer 11 and n^- single crystal island 61 are partially connected with each other. And the parts of p^{++} layer 11 kept in contact with single crystal island 61, which has a low impurity concentration, provide a high hole injection efficiency. Thus, the modification of Figs. 8A and 8B permit a larger current to flow then in the case where n^+ layer 31 is formed on the entire p^{++} layer 11.

Fig. 3 is a vertical sectional view of another modification of the second embodiment of the present invention. In Fig. 3, the same reference symbols as in Fig. 1 refer to the same or equivalent parts in Fig. 1. The structure of this modification is different from that of the embodiment of Fig. 2 in that p^{++} layer 11 and n^- single crystal island 61 are short-circuited by collector electrode 4 in their surface and also an n^+ buried layer 33 is short-circuited with p^{++} layer 11 by collector electrode 61 through n^- single crystal island in the substrate surface. In the embodiment of Fig. 2, the short-circuiting effect is so great that the injection efficiency of holes is reduced and thus the conductivity modulation may be insufficient. In this modification, n^+ embedded layer 33 is short-circuited with p^{++} layer 11 by collector electrode 4 through single crystal island 61 which has high resistance so that the amount of the electrons flowing from n^+ embedded layer 33 to collector electrode 4 is reduced. Thus, the injection of holes from p^{++} layer 11 is increased, thereby permitting a larger current to flow than in the structure of Fig. 2. The same effect can also be obtained by forming a Schottky junction between collector electrode 4 and n^- layer 61.

Fig. 4 is a vertical sectional view of still another modification of the second embodiment of the present invention. In Fig. 4, the same reference symbols as in Fig. 1 refer to the same or equivalent parts in Fig. 1. The structure of this modification is different from that of Fig. 3 in that an n^+ layer 34 and a p^+ layer 12 are formed in the surface of n^- single crystal island 61 and an n^- layer 51 is formed between n^+ embedded layer 33 and n^+ layer 34. The provision of n^+ layer 34 permits the contact resistance for collector electrode 4 to be reduced. The p^+ layer 12 formed in the neighborhood of the surface of n^- single crystal island 61 permits the electrons directly reaching n^+ layer 34 to be reduced and the electric field to be reduced. Further, by varying the impurity concentration of n layer 51, the amount of electrons flowing n^+ embedded layer 33 to collector electrode 4 via n layer 51 can be varied. More specifically, if the impurity concentration of n layer 51 is increased, the amount of electrons flowing to collector electrode 4 via n layer 51 is increased so that the injection of holes from p^+ layer 11 can be restricted. By controlling the injection of holes from p^{++} layer 11 in this manner, the switching speed and the current density of the device can be advantageously controlled.

Fig. 5 is a vertical sectional view of a further modification of the second embodiment of the present invention. In Fig. 5, the same reference symbols as in Fig. 1 refer to the same or equivalent parts in Fig. 1. The structure of this modification is different from that of Fig. 2 in that an n^+ layer 52 in place of n^+ layer 31 is formed between p^{++} layer 11 and n^- single crystal island 61 so as to surround n^- single crystal island 61, in that an n^- layer 53 in contact with n^+ layer 52 is formed so as to be exposed to the surface of n^- single crystal island 61 and a p^+ layer 41′ is formed within the n^- layer 53 so as to be exposed to the surface and be in contact with n^+ layer 52, and in that a gate insulator 8 of an insulating film is provided on the surface of n^+ layer 52 to be also extended onto p^+ layer 41 and p^{++} layer 11 and a second gate G_2 is provided by stacking an electrode material on the gate insulator 8. In operation, if a positive potential is applied to the first gate G, electrons flow out from n^+ layer 32 thereby to turn the device on. On the other hand, if the potential applied to the first gate G is removed, the injection of electrons from n^+ layer 32 stops. Then, if the second gate G_2 is placed in a lower potential state than the collector electrode, the polarity of n^+ layer 52 below gate insulator 8 is inverted. Thus, p^+ layer 42 is short-circuited with p^{++} layer 11 so that electrons can be extracted out from n^- single crystal island 62 through n^- layer 53, a short- circuiting electrode 7, p^+ layer, n^+ layer 52, p^{++} layer 11 and the collector electrode, which permits the device to be turned off at a high speed. In this way, in turning on the IGBT device, the electrons are extracted out by placing the second gate G_2 in the conduction state so that the device can be turned off at a high speed.

Fig. 6A is a vertical sectional view of a third embodiment of the present invention. Fig. 6B is a

sectional view taken on line a-a′ of Fig. 6A. In Figs. 6A and 6B, the same reference symbols as in Fig. 1 refer to the same or equivalent parts in Fig. 1. In this embodiment, an n^{++} short-circuiting layer 21 and p^{++} layer 11 are formed from inter-layer insulating film 1 toward n^- single crystal island 61. n^{++} short-circuiting layer 21 and p^{++} layer 11 are short-circuited by collector electrode 4 in their surface. Further, p^{++} layer 11 is partially removed so that n^{++} short-circuiting layer 21 and n^- single crystal island 61 are partially kept in contact with each other. Thus, by varying the area where n^{++} short-circuiting layer 21 and n^- single crystal island 61 are kept in contact with each other, the amount of electrons flowing from n^- single crystal island 61 to collector electrode 4 via n^{++} short-circuiting layer 21 is varied so that the amount of holes injected from p^{++} layer 11 can be controlled. Further, the n^{++} short-circuiting layer 21 formed immediately below the gate electrode G, which serves to extract electrons, permits a current to uniformly flow in the vertical direction and hence a large current to flow. This also prevents the device from being latched up.

Fig. 7A is a vertical sectional view of a modification of the third embodiment of the present invention. Fig. 7B is a sectional view taken on line a-a′ of Fig. 7A. In Figs. 7A and 7B, the same reference symbols as in Fig. 1 refer to the same or equivalent parts in Fig. 1. In this embodiment, an n^+ layer 34 is formed between p^{++} layer 11 and n^- single crystal island 61. The p^{++} layer 11 is partially removed so that n^- single crystal island 61 is short-circuited with p^{++} layer 11 through n^+ layer 34 and n^{++} short-circuiting layer 21. The provision of n^+ layer 34 serves to shorten the lifetime of minority carriers thereby enhancing the switching speed, and also prevent the depletion layer from punch-through effect in p^{++} layer 11 to reduce the breakdown voltage.

It goes without saying that in the several embodiment as explained above, replacing the conduction type of each layer (from the n type to the p type and vice versa) gives the same effect.

In the above explanation, the n^- layer n layer, n^+ layer and n^{++} layer denote n^- type layers which have a higher impurity concentration in this order. Likewise, the p^- layer, p layer, p^+ layer and p^{++} layer denote p^-type layers which has a higher impurity concentration in this order.

The typical doping concentration (the number of dopant atoms per a unit volume 1 cm^3) of each of the layers are roughly as follows.

(1) The p^{++} layer which serves as a collector layer: 1×10^{18} - 1×10^{20}

(2) The active base region (the n^- single crystal island which serves as a drift region): 1×10^{13} -5×10^{15}

(3) The p layer which serves as a shield base region (channel): 1×10^{15} - 5×10^{18}

(4) The n^+ layer which serves as a cathode region (emitter region): larger than 1×10^{19}

Although in the above explanation of the respective embodiments, the so-called dielectric isolation substrate using a polycrystal silicon as a supporting substrate has been used, any other structure may be uses as long as isolation between the single crystal islands is maintained. Further, a plurality of single crystal islands may be formed on the supporting substrate, and the device of the present invention and the other function devices may be formed in each single crystal island so that an IC (integrated circuit) for a large current is constituted.

As understood from the above explanation, in accordance with the present invention, IGBT can be formed within a semiconductor island surrounded by an insulating film and dielectrically isolated from the other islands so that current can flow in the vertical direction. This permits a current to uniformly flow in the vertical direction and hence a large current to flow. Further, the amount of holes traversing the short-circuiting resistance of the n^+ layer can be reduced so that the latch-up can be prevented. Moreover, short-circuit the p layer and n layer formed in the collector layer by the collector electrode permits the device to be operated at a high speed.

The present invention is summarized as follows. A dielectric isolation substrate is used as a supporting substrate. An island-shaped second semiconductor region of a second conduction type is formed so as to be surrounded by an insulator and a first semiconductor layer of a first conduction type. An FET having an insulated gate is formed in the second semiconductor region. A collector electrode is attached to the first semiconductor layer.

In accordance with the present invention, a semiconductor device which is suitable for integration and can performing a switching operation of a large electric power can be provided.

Claims

1. A semiconductor device comprising:
a supporting substrate (2);
a plurality of single crystal island regions (61) which are formed is said supporting substrate (2) by electric isolation means (1);
a first region (61) of one conduction type formed in each of said island regions, said first region being extended in the island region from its surface;
a second region (41) of the other conduction type formed in said first region (61) and having a higher

impurity concentration than said first region (61), said second region (41) being extended int he island region from its surface and forming a first pn junction with said first region (61);
a third region (32) of one conduction type formed in said second region (41) and having a higher impurity concentration than said second region (41), said third region (32) being extended in the island region from its surface and forming a second pn junction with said second region (41);
a fourth region (11) of the other conduction type located between said first region (61) and said isolation means (1) and having a higher impurity concentration than said first region (61), said fourth region (11) having an exposed surface exposed to the surface of said island region;
a first main electrode (E) located on said island region surface and kept in ohmic contact with said second and third regions (41, 32);
a second main electrode (C) located on said island region surface and kept in ohmic contact with the exposed surface of said fourth region (11); and
a control electrode (G) located on said island surface through an insulating film (6) and extended over said first, second and third regions (61, 41, 32).

2. A semiconductor device according to Claim 1, wherein said electric isolation means (1) is a dielectric film.

3. A semiconductor device according to Claim 1, further comprising a fifth region (31, 52) of one conduction type formed between said first region (61) and said fourth region (11) and having an impurity concentration higher than said first region (61) and lower than said fourth region (11).

4. A semiconductor device according to Claim 3 , further comprising
a sixth region (53) of one conduction type being in contact with said fifth region (52) and exposed to said island region surface, said sixth region (53) having a higher impurity concentration than said first region (61);
a seventh region (41′) of the other conduction type formed in said sixth region (53) so as to be in contact with said fifth region (52) and to be exposed to said island region surface, said seventh region (41′) having a higher impurity concentration than said sixth region (53);
a second control electrode (G_2) located on said island region surface through an insulator (8) and extended over said fourth region (11), said fifth region (52) and said seventh region (41′); and
a short circuiting electrode (7) located on said island region surface and kept in ohmic contact with said sixth region (53) and said seventh region (41′).

5. A semiconductor device comprising:
a supporting substrate (2);
a plurality of single crystal island regions (61) which are formed in said supporting substrate (2) by electric isolation means (1);
a first region (61) of one conduction type formed in each of said island regions, said first region (61) being extended in the island region from its surface;
a second region (41) of the other conduction type formed in said first region (61) and having a higher impurity concentration than said first region (61), said second region (41) being extended in the island region from its surface forming a first pn junction with said first region (61);
a third region (32) of one conduction type formed in said second region (41) and having a higher impurity concentration than said second region (41), said third region (32) being extended in the island region from its surface and forming a second pn junction with said second region (41);
a fourth region (11) of the other conduction type located between said first region (61) and said isolation means (1) and having a higher impurity concentration than said first region (61), said fourth region (11) having an exposed surface exposed to the surface of said island region;
a first main electrode (E) located on said island region surface and kept in ohmic contact with said second and third regions (41, 32);
a second main electrode (C) located on said island region surface and kept in ohmic contact with the exposed surface of said fourth region (11) and said first region (61); and
a control electrode (G) located on said island surface through an insulating film (6) and extended over said first, second and third regions (61, 41, 32).

6. A semiconductor device according to Claim 5, wherein said electric isolation means (1) is a dielectric film.

7. A semiconductor device according to Claim 5, further comprising a fifth region (33) of one conduction type formed between said first region (61) and said fourth region (11) so as to be located at only the bottom of said island region and having an impurity concentration higher than said first region (61) and lower than said fourth region (11).

8. A semiconductor device comprising:
a supporting substrate (2);
a plurality of single crystal island regions (61) which are formed in said supporting substrate (2) by electric isolation means (1);
a first region (61) of one conduction type formed in each of said island regions, said first region (61) being extended in the island region from its surface;
a second region (41) of the other conduction type

formed in said first region (61) and having a higher impurity concentration than said first region (61), said second region (41) being extended in the island region from its surface and forming a first pn junction with said first region (61);
a third region (32) of one conduction type formed in said second region (41) and having a higher impurity concentration than said second region (41), said third region (32) being extended in the island region from its surface and forming a second pn junction with said second region (41);
a fourth region (11) of the other conduction type located between said first region (61) and said isolation means (1) and having a higher impurity concentration than said first region (61), said fourth region (11) having an exposed surface exposed to the surface of said island region;
a fifth region (31) of one conduction type formed between said first region (61) and said fourth region (11) and having an impurity concentration higher than said first region (61) and lower than said fourth region (11), said fifth region (31) having an exposed surface on the surface of said island region;
a first main electrode (E) located on said island region surface and kept in ohmic contact with said second and third region (41, 32);
a second main electrode (C) located on said island region surface and kept in ohmic contact with the exposed surfaces of said fourth region (11) and said fifth region (31); and
a control electrode (G) located on said island surface through an insulating film (6) and extended over said first, second and third regions (61, 41, 32).

9. A semiconductor device according to Claim 8, wherein said electric isolation means (1) is a dielectric film.

10. A semiconductor device according to Claim 8, wherein said fifth region (31) is selectively removed at plural portions of the bottom of said island region where said first region (61) and said fourth region (11) are adj acent to each other.

11. A semiconductor device comprising:
a supporting substrate (2);
a plurality of single crystal island regions which are formed in said supporting substrate by electric isolation means (1);
a first region (61) of one conduction type formed in each of said island regions, said first region (61) being extended in the island region from its surface;
a second region (41) of the other conduction type formed in said first region and having a higher impurity concentration than said first region (61), said second region (41) being extended in the island region from its surface and forming a first pn junction with said first region (61);
a third region (32) of one conduction type formed in said second region (41) and having a higher impurity concentration than said second region (41), said third region (32) being extended in the island region from its surface and forming a second pn junction with said second region (41);
a fourth region (21) of one conduction type located between said first region (61) and said isolation means (1) and having a higher impurity concentration than said first region (32), said fourth region (21) having an exposed surface exposed to the surface of said island region;
a fifth region (11) of the other conduction type located between said first region (61) and said fourth region (21) and having a higher impurity concentration than said first region (61), said fifth region (11) having an exposed surface exposed to said island region surface and being selectively removed at plural portions of the bottom of said island region where said first region (61) and said fourth region (21) are adjacent to each other;
a first main electrode (E) located on said island region surface and kept in ohmic contact with said second and third regions (41, 32);
a second main electrode (C) located on said island region surface and kept in ohmic contact with the exposed surfaces of said fourth region (21) and said fifth region (11); and
a control electrode (G) located on said island region surface through an insulating film (6) and extended over said first, second and third regions (61, 41, 32).

12. A semiconductor device according to Claim 11, wherein said electric isolation means (1) is a dielectric film.

13. A semiconductor device comprising
a supporting substrate (2);
a plurality of single crystal island regions which are formed in said supporting substrate (2) by electric isolation means (1);
a first region (61) of one conduction type formed in each of said island regions, said first region(61) being extended in the island region from its surface;
a second region (41) of the other conduction type formed in said first region (61) and having a higher impurity concentration than said first region (61), said second region (41) being extended in the island region from its surface and forming a first pn junction with said first region (61);
a third region (32) of one conduction type formed in said second region (41) and having a higher impurity concentration than said second region (41), said third region (32) being extended in the island region from its surface and forming a second pn junction with said second region (41);
fourth (34), fifth (11) and sixth (21) regions located successively from the first region side between

said first region (61) and said electric isolation means (1), said fourth region (34) of one conduction type having a higher impurity concentration than said first region (61) and an exposed surface exposed to the island region surface, said sixth region (21) of one conduction type having a higher impurity concentration than said fourth region (34) and an exposed surface exposed to the island region surface, said fifth region (11) of the other conduction type having a higher impurity concentration than said fourth region (34) and an exposed surface exposed to the island region surface and being selectively removed at plural portions of the bottom of said island region were said fourth region (34) and said sixth region (21) are adjacent to each other;

a first main electrode (E) located on said island region surface and kept in ohmic contact with said second and third regions (41, 32);

a second main electrode (C) located on said island region surface and kept in ohmic contact with the exposed surfaces of said fifth region (11) and said sixth region (21); and

a control electrode (G) located on said island region surface through an insulating film (6) and extended over said first, second and third regions (61, 41, 32).

14. A semiconductor device according to Claim 13. Wherein said electric isolation means is a dielectric film.

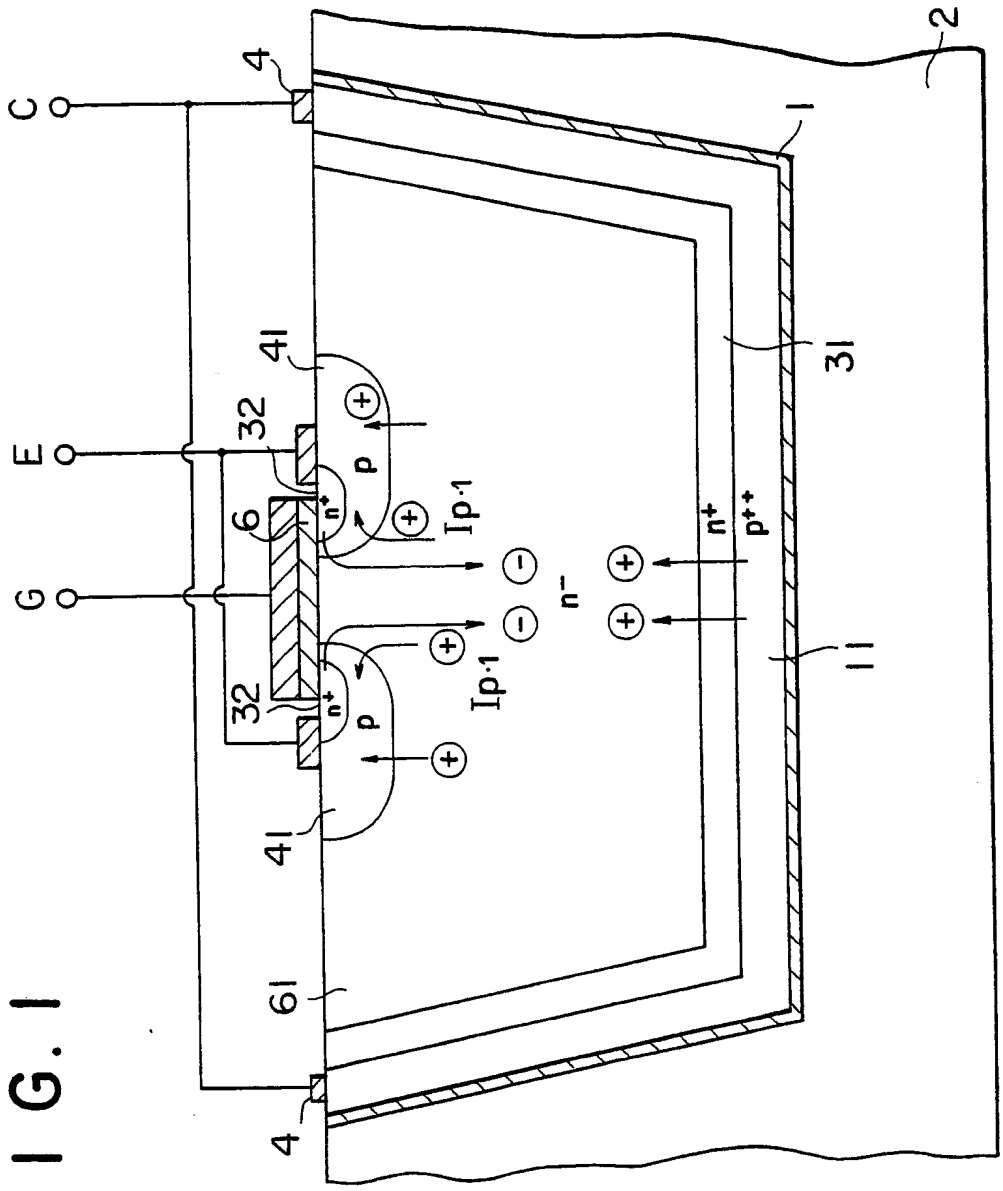


FIG. 1

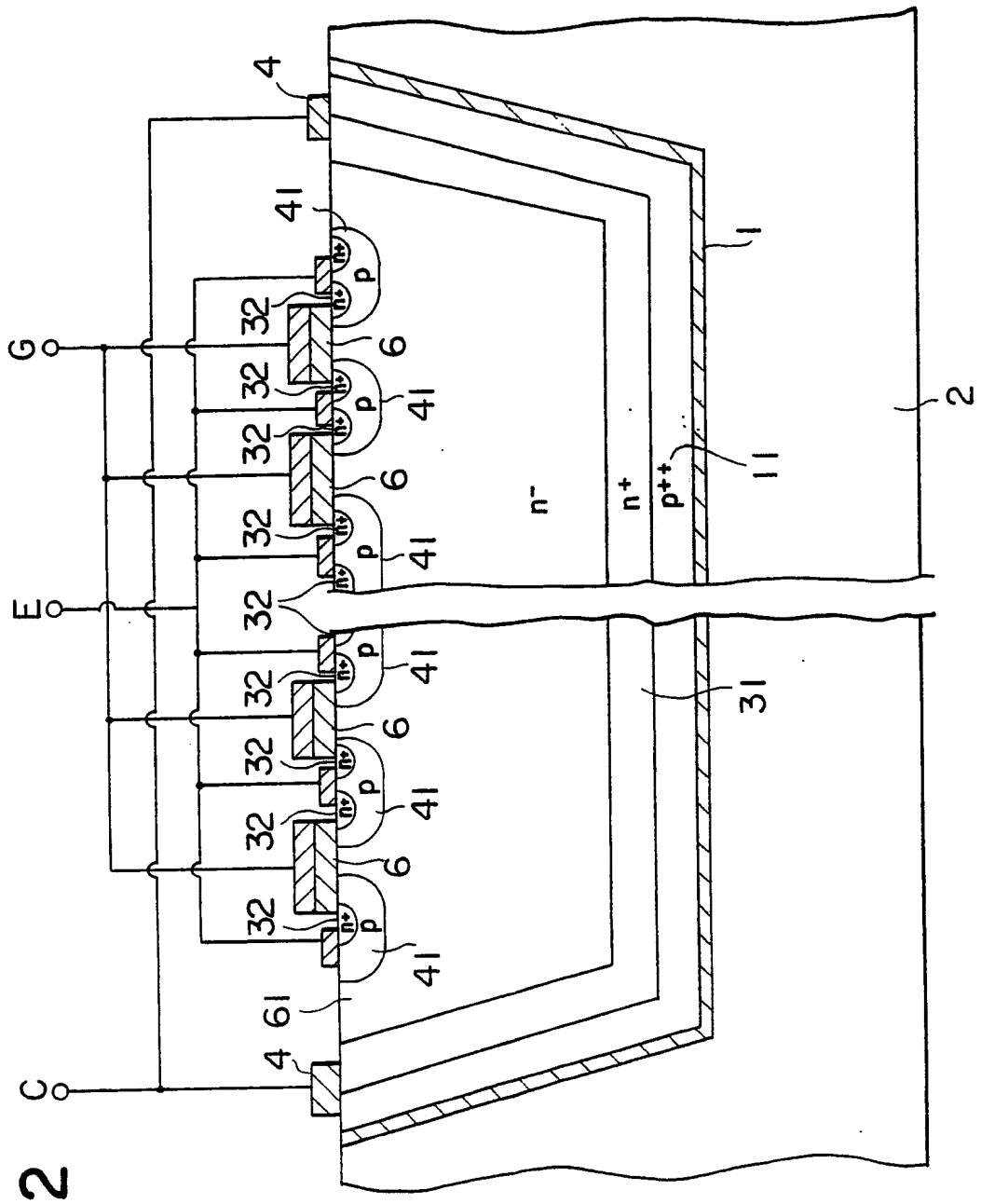


FIG. 2

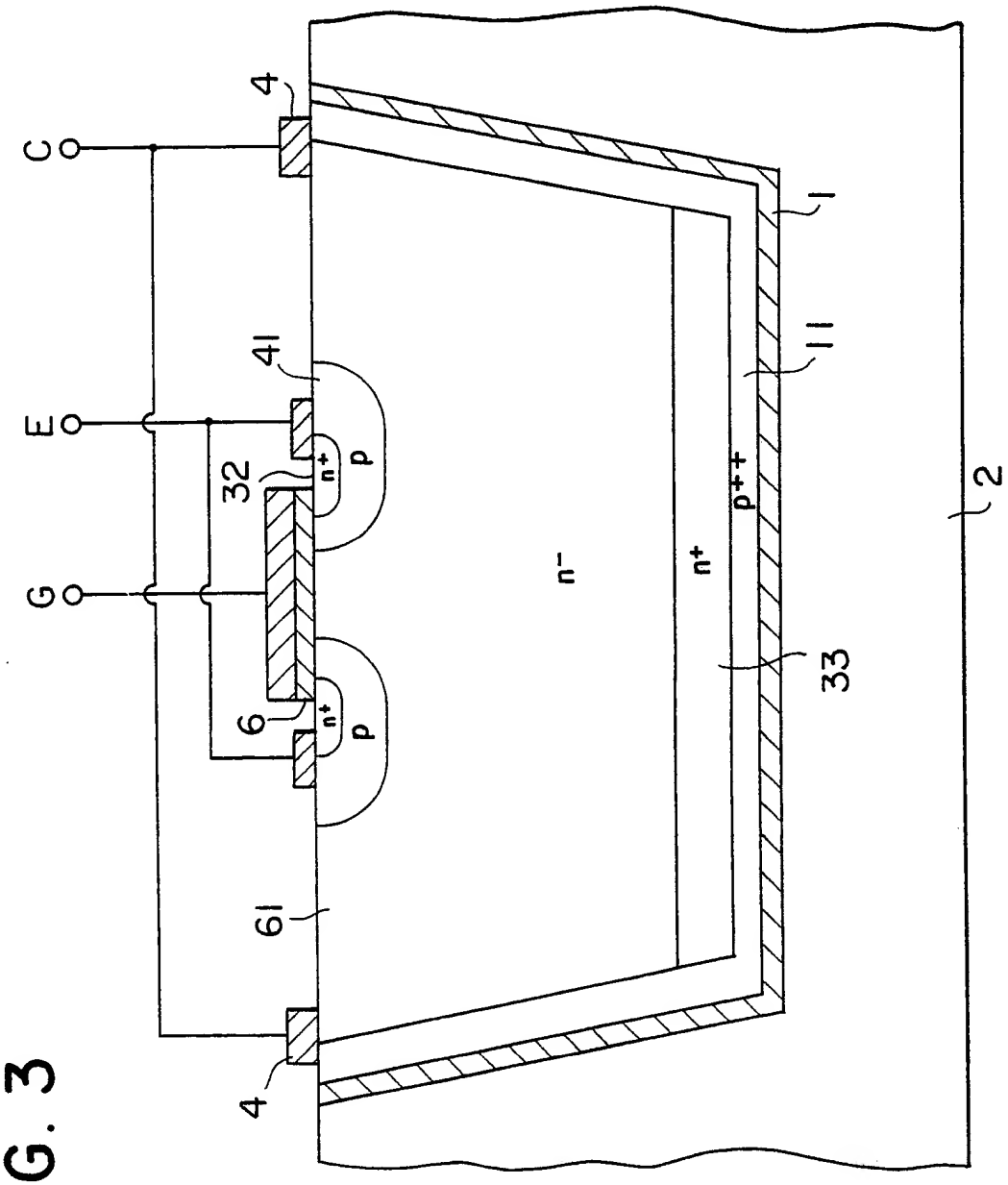


FIG. 3

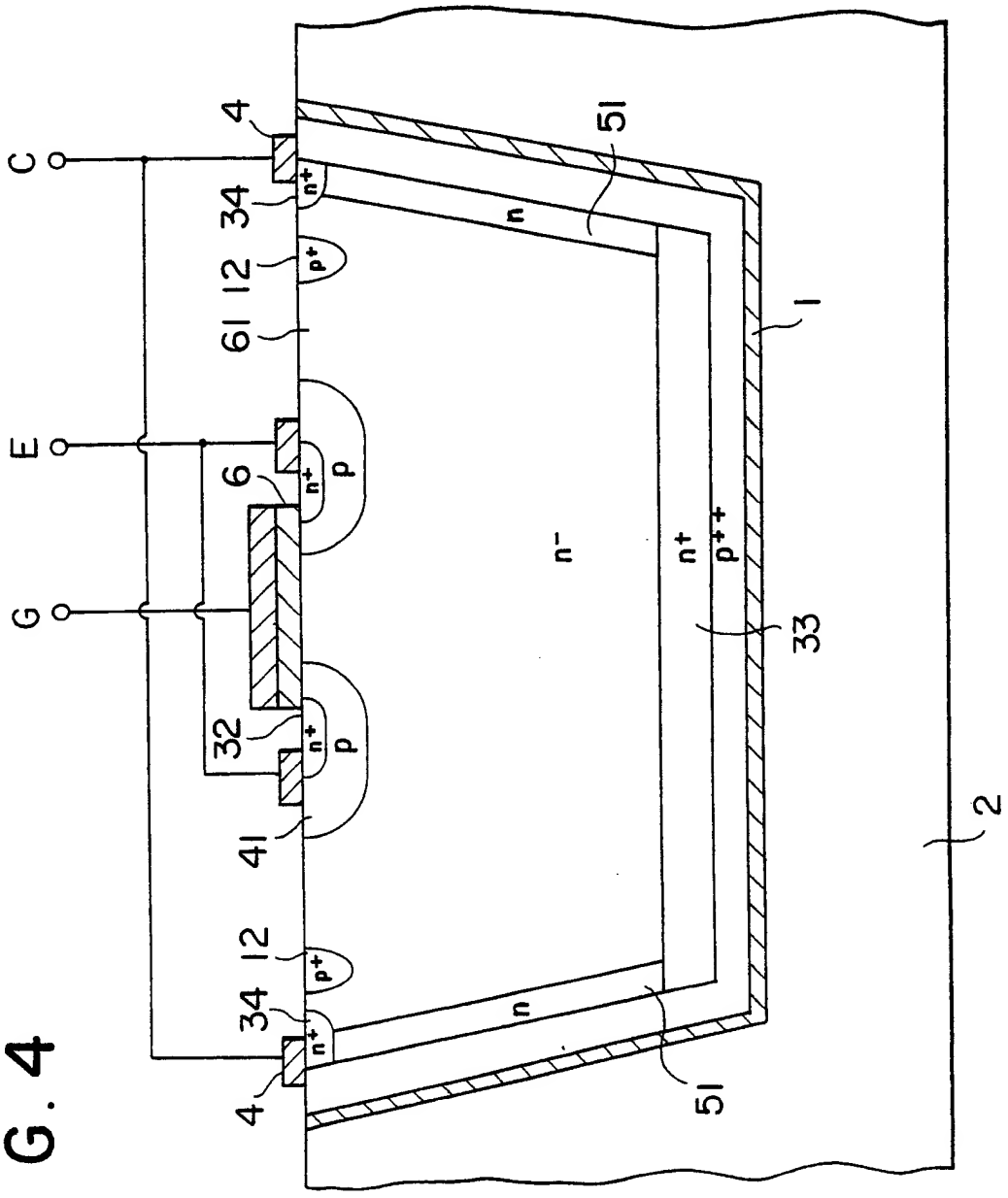


FIG. 4

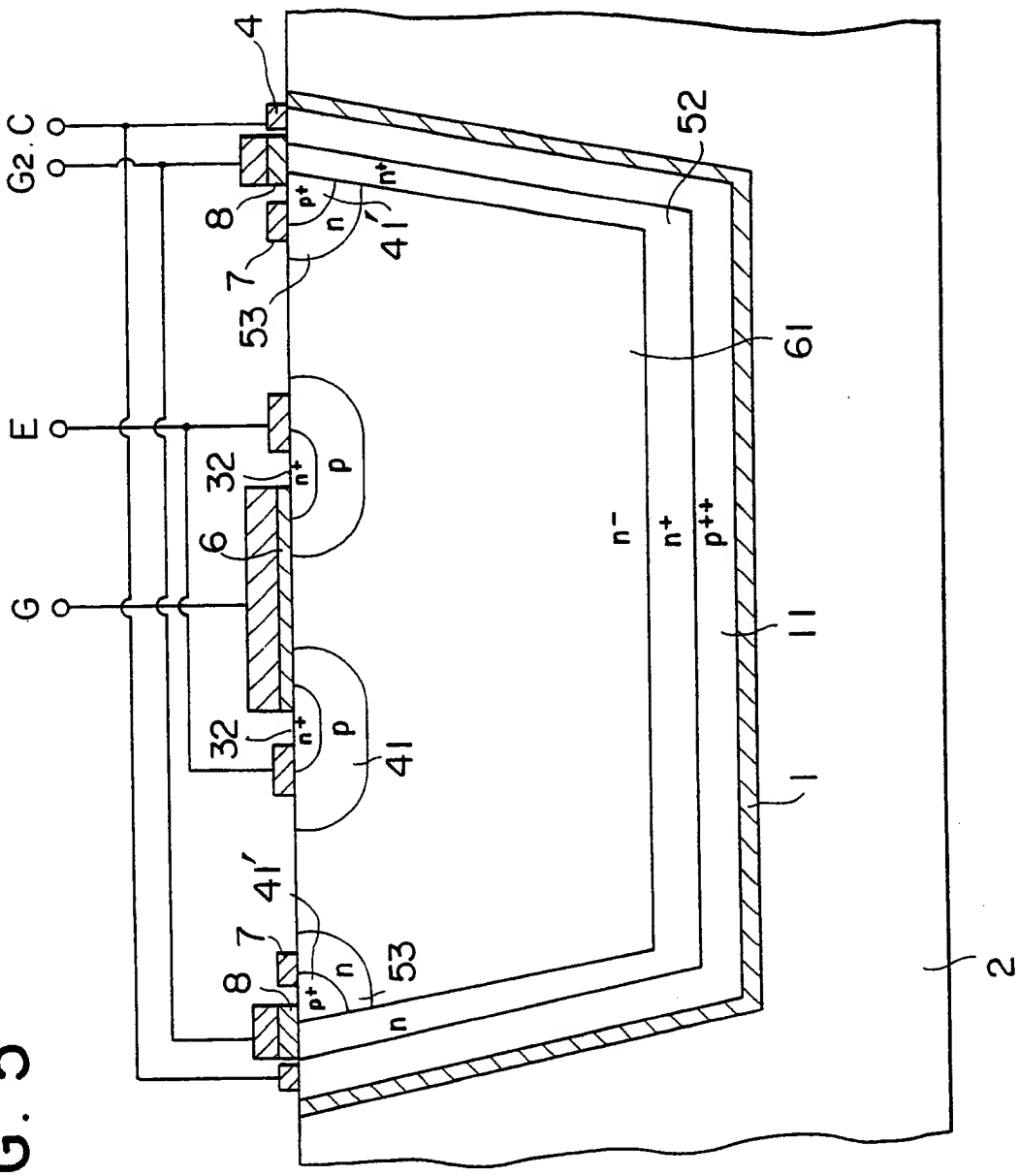


FIG. 5

FIG.6A

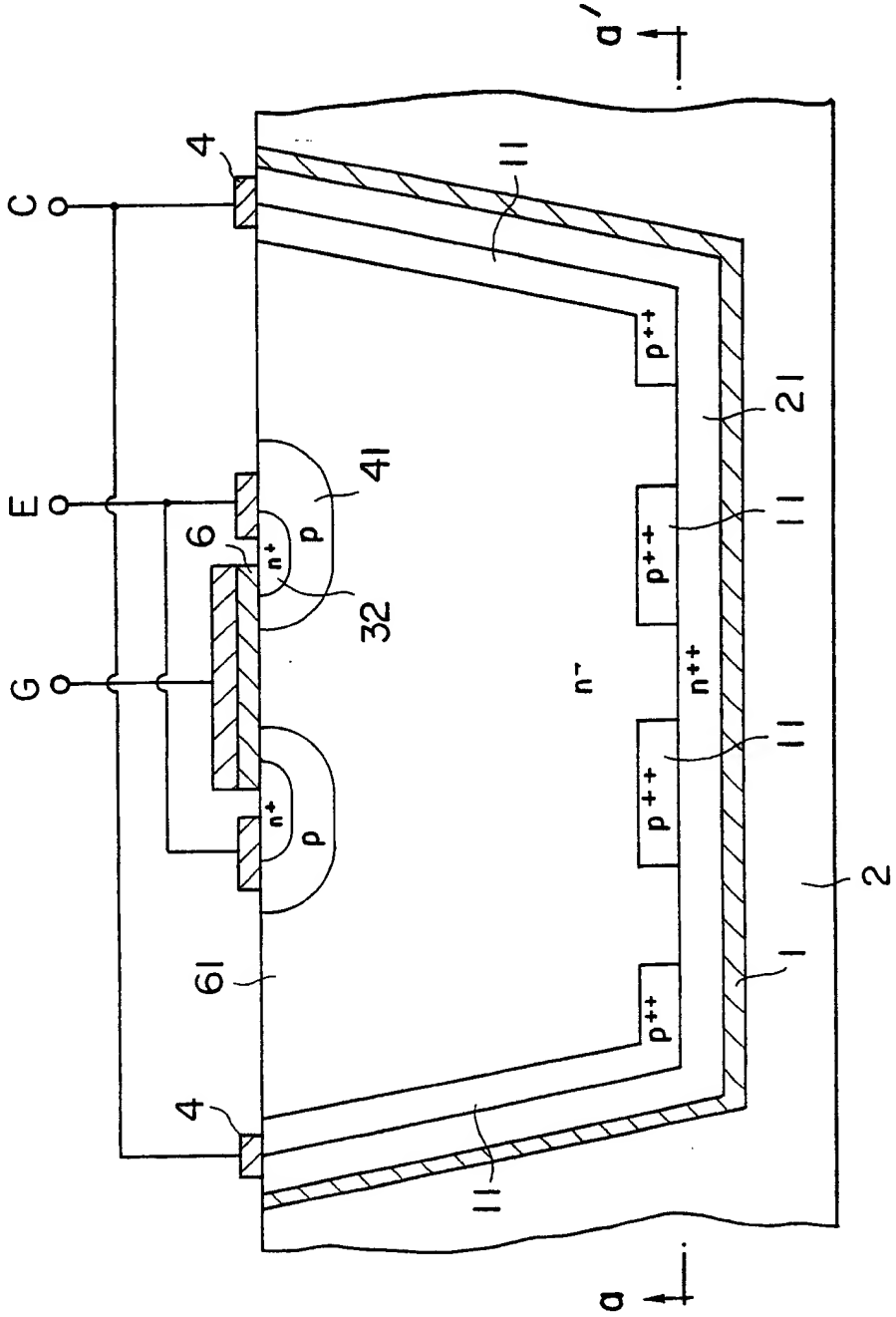


FIG.6B

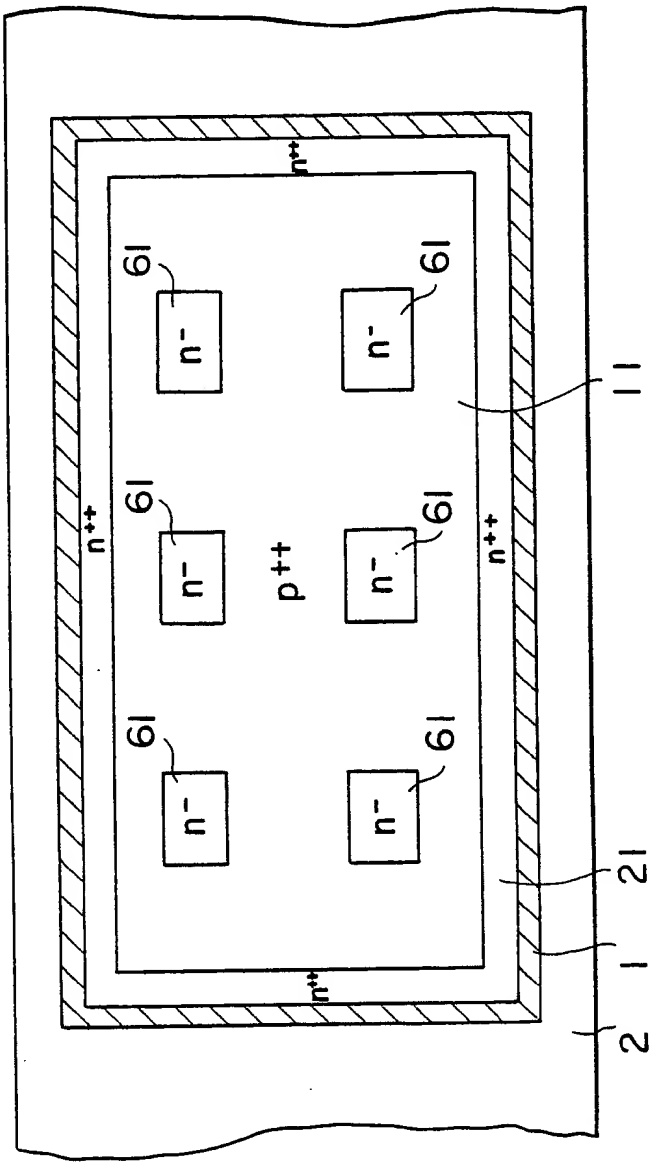


FIG. 7A

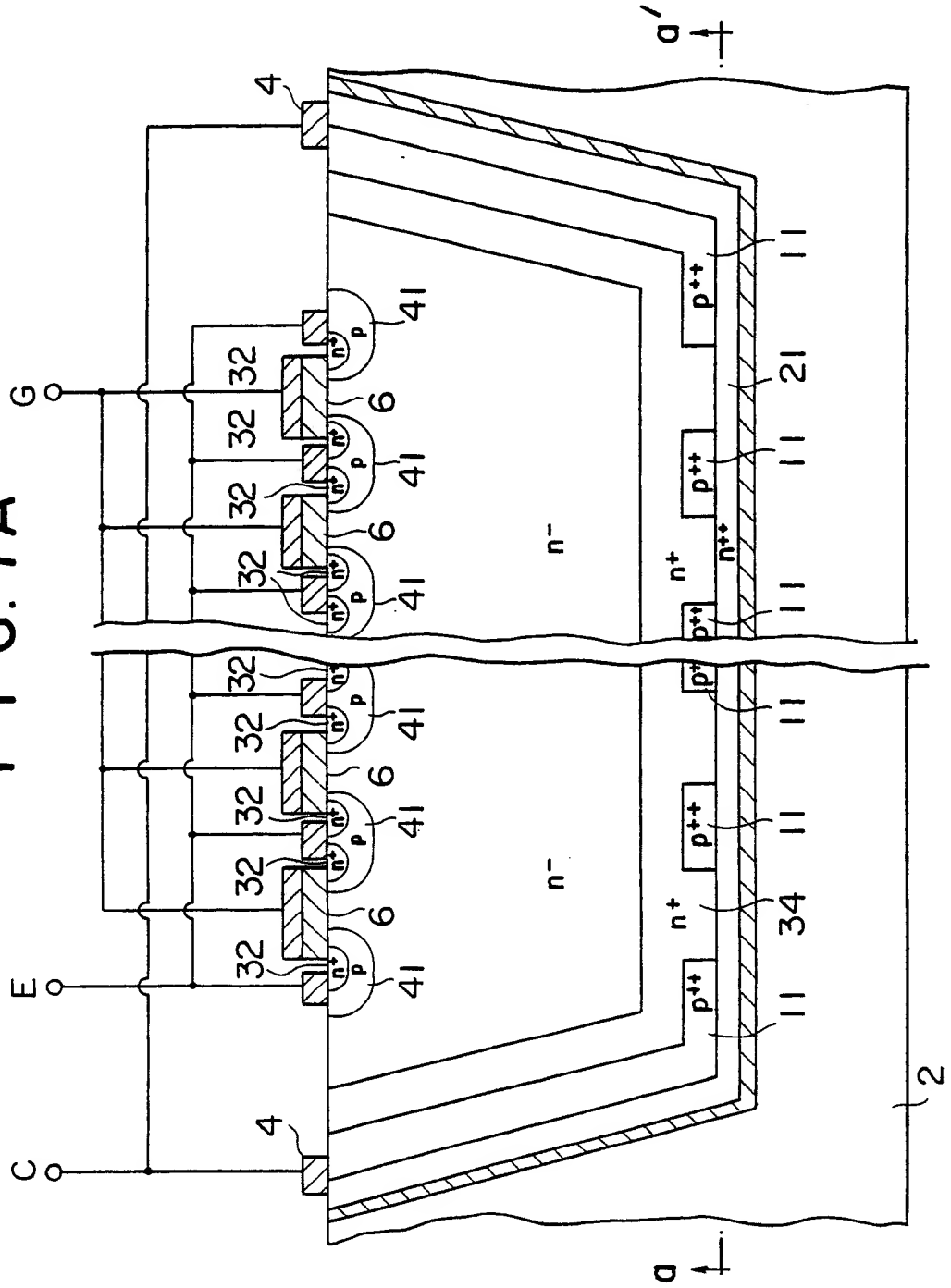


FIG. 7B

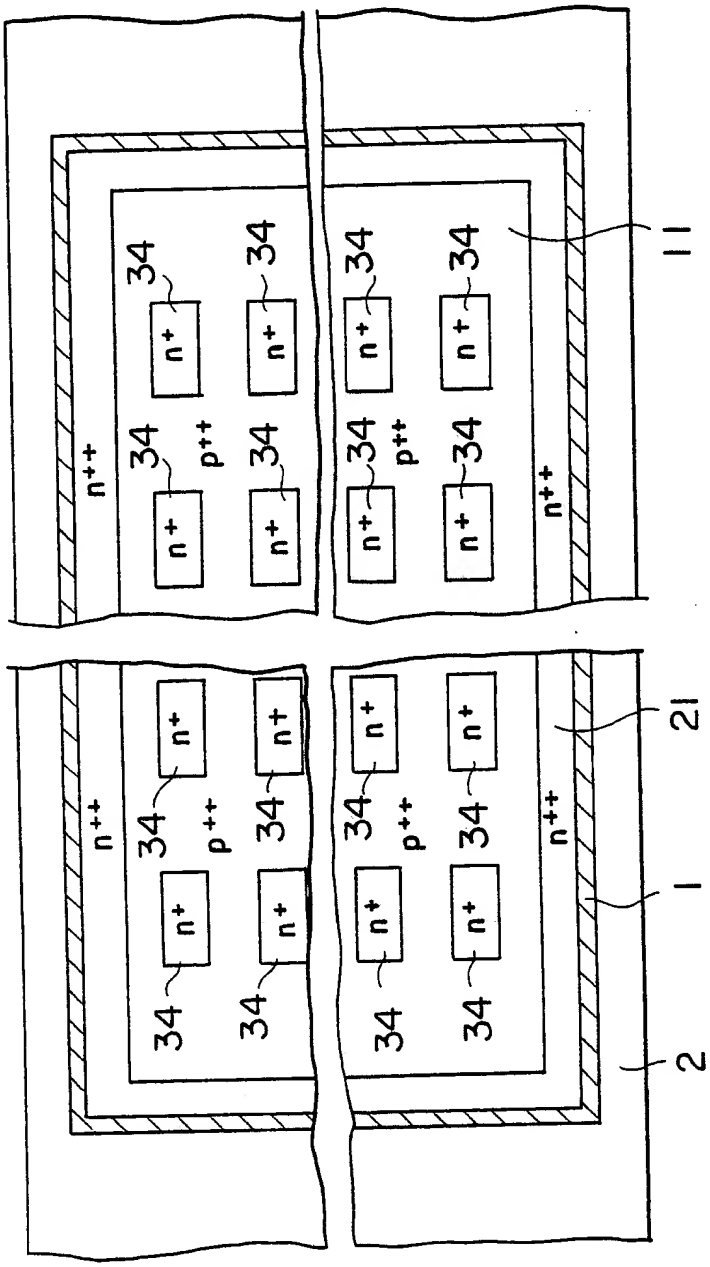


FIG.8A

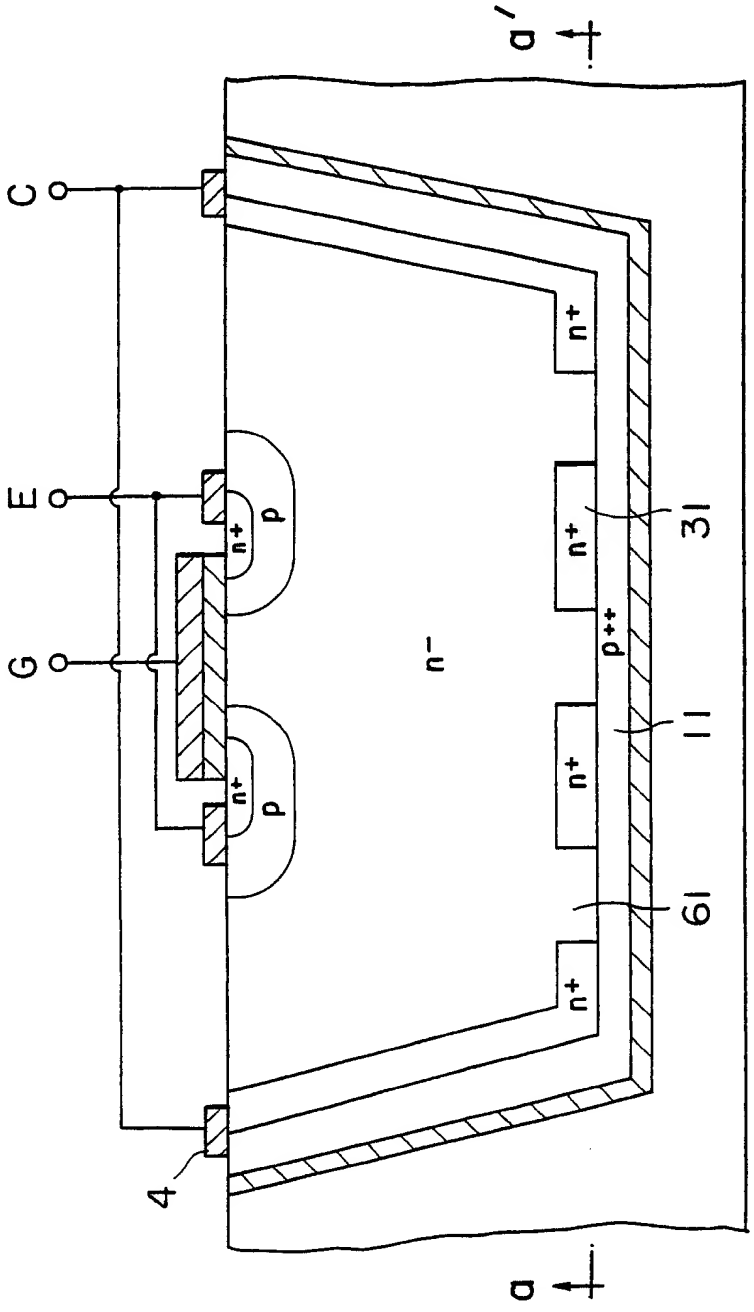


FIG. 8B

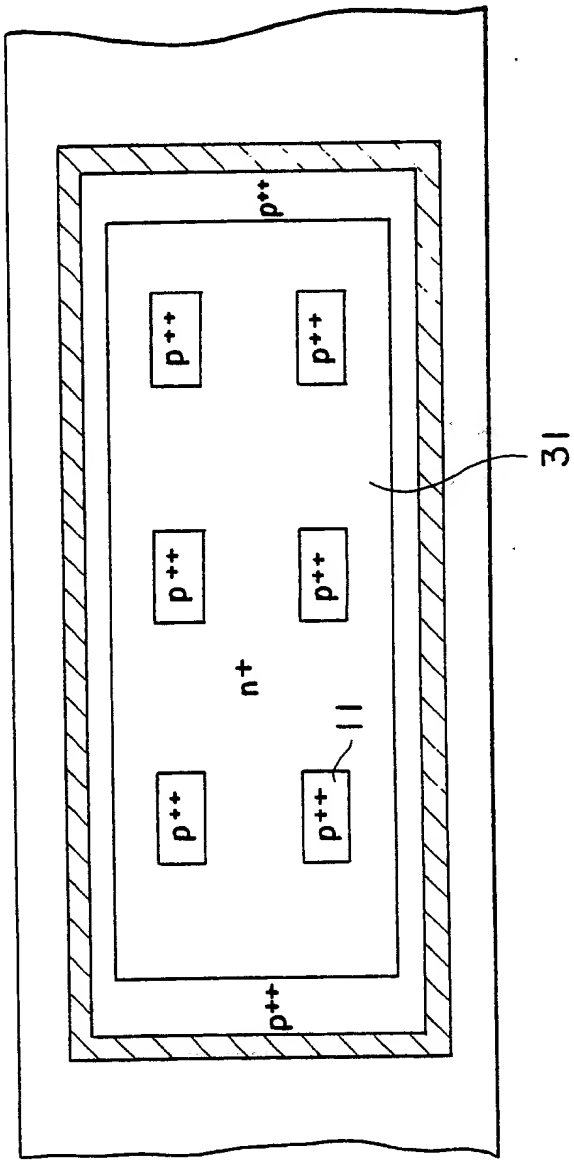
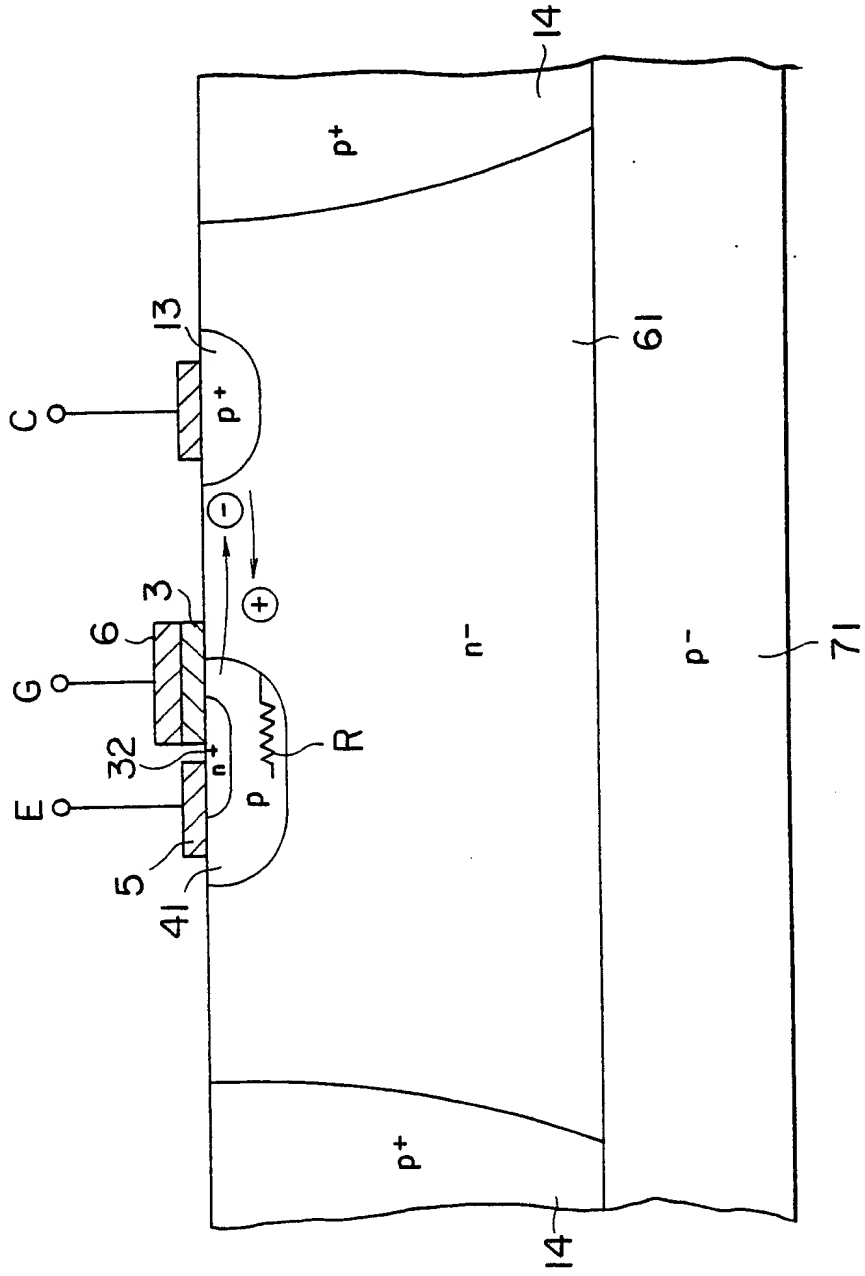


FIG. 9
PRIOR ART



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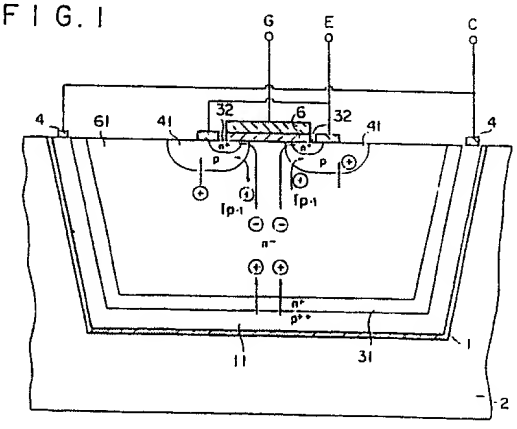
(54) **Insulated gate bipolar transistor.**

(57) An insulated gate bipolar transistor (IGBT) permits a large current to uniformly flow. A plurality of single crystal island regions (61) are formed in a supporting substrate (2) using dielectric films (1). Formed in each of the island regions are an n^- first region (61), a p second region (41) within the first region, an n^+ third region (32) within the second region (41) and a p^{++} fourth region (11) between the first region (61) and the dielectric film. All of these regions are exposed to the surface of the island region. Formed on the surface of the island region are a first main electrode (E) kept in ohmic contact with the second (41) and third (32) regions, a second main electrode (C) kept in ohmic contact with the fourth region (11) and a control electrode (G) located on the second (41) and third region (32) through an insulator (6).

FIG. 1



EP 0 338 312 A3

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EUROPEAN SEARCH REPORT

Application Number

EP 89 10 5833

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	TECHNICAL DIGEST OF THE INTERNATIONAL ELECTRON DEVICES MEETING, Washington, DC, 1st-4th December 1985, pages 724-727, IEEE, New York, US; H.W. BECKE: "Approaches to isolation in high voltage integrated circuits" * Page 726, right-hand column; figure 7 * ---	1,2,5,6 ,11-14	H 01 L 29/72 H 01 L 29/08 // H 01 L 27/12
A	ELECTRO AND MINI/MICRO NORTHEAST, New York, 23rd-25th April 1985, pages 1-3, New York, US; P.W. SHACKLE: "Custom high voltage integrations for industry" * Figures 1,3 * ---	1-3,5,6 ,8,9,11 -14	
A	GB-A-2 088 631 (GENERAL ELECTRIC CO.) * Figure 13 * & JP-A-57 120 369 (Cat. D,A) ---	1,3,7,8 ,11,13	
A	PATENT ABSTRACTS OF JAPAN, vol. 10, no. 175 (E-413)[2231], 20th June 1986; & JP-A-61 24 278 (TOSHIBA K.K.) 01-02-1986 * Abstract; figures * ---	5	TECHNICAL FIELDS SEARCHED (Int. Cl.4) H 01 L
A	PATENT ABSTRACTS OF JAPAN, vol. 10, no. 129 (E-403)[2186], 14th May 1986; & JP-A-60 260 152 (NIPPON DENKI K.K.) 23-12-1985 * Abstract; figures * ---	1,3,7,8 ,10	
	EP-A-0 111 804 (GENERAL ELECTRIC CO.) * Page 17, line 19 - page 19, line 29; figures 3,4 * --- -/-	1,4	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29-11-1989	MORVAN D.L.D.

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Application Number

EP 89 10 5833

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	EP-A-0 111 803 (GENERAL ELECTRIC CO.) * Figure 2 * & JP-A-59 132 667 (Cat. D,A)	8,11,13	
			TECHNICAL FIELDS SEARCHED (Int. Cl.4)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29-11-1989	MORVAN D.L.D.

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